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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/046,566	CHOW, FELIX	
	Examiner	Art Unit	
	Robert C. Scheibel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-13,15 and 37-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-13,15 and 37-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Examiner acknowledges receipt of Applicant's Amendment filed 3/2/2007.
- Claims 1-4, 6, 8, 10-13, 15, 37, and 42-50 are currently amended.
- Claims 5, 7, and 14 are cancelled with this amendment.
- Claims 1-4, 6, 8-13, 15, and 37-50 are currently pending.

Response to Arguments

1. Applicant's arguments, see "Objections to the Claims" on page 13, filed 3/2/2007, with respect to the objections to claims 44 and 47 have been fully considered and are persuasive. The objection to claims 44 and 47 has been withdrawn.

2. Applicant's arguments, see "35 U.S.C. 103" on pages 13-18, filed 3/2/2007, with respect to the rejection of claims 1-15 and 37-50 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive.

In the first 3 paragraphs of this section, Applicant summarizes the three groups of rejections under 35 U.S.C. 103(a). On pages 14-16, Applicant addresses the rejection of claim 1. In the first paragraph on page 14, Applicant recites various limitations of claim 1. In the next paragraph, Applicant argues that Trippe and Stephenson fail to describe these limitations. Specifically, Applicant argues that Trippe describes an HDLC receive that processes eight bits in parallel. While this may be true in some exemplary embodiments, Trippe clearly indicates that the framer may be configured to process 2^n bits in parallel. Clearly, this includes 16 bits or 2 bytes as recited in claim 1. Trippe refers to the bits being processed in parallel as a "group of

bits" throughout, and it is clear that an eight bit group is merely one example size for this group of bits. Applicant cites paragraph 43 of Trippe and asserts that the accumulator described here is required because the receiver processes only eight bits at a time. However, this is misleading as Trippe clearly states that "frame flags may straddle different ***groups of bits***", which were clearly indicated as including 2^n bits in paragraph 26 as stated above. In the next paragraph, Applicant asserts that Trippe fails to disclose "storing two bytes of HDLC data in a shift register and processing two bytes of data within a shift register with a plurality of comparators coupled with a shift register" as required by claim 1. However, the rejection relies upon Stephenson, Jr. to disclose the limitation that these two bytes are stored in a shift register and the limitations of the comparators. However, the Trippe reference would clearly process 2n bits in one clock cycle and thus the limitations of detecting a start-of-frame sequence in first clock cycle and an end-of-frame sequence in a subsequent sequence are clearly disclosed.

In the next few paragraphs, Applicant argues that Stephenson, Jr. fails to disclose the limitation of storing two bytes of HDLC data in a shift register. Applicant cites a section of Stephenson, Jr. which indicates conversion of data to 8 bit parallel data and seems to suggest that this implies that only 8 bits are processed at a time. However, this merely discloses that 8 bits are shifted into the shift register (which is the three sequential latches) at a time. Stephenson, Jr. modifies Trippe (which as described above, already discloses processing 2 bytes in parallel) to disclose the limitations of the comparators and shifting in/out one byte per clock cycle.

Applicant argues that claims 2-4 are allowable as they are dependent upon claim 1. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claims 44 and 47 are allowable as they contain limitations similar to claim 1. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claims 45 and 46 are allowable as they are dependent upon claim 44. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claims 48-50 are allowable as they are dependent upon claim 47. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

On page 17, Applicant recites portions of claim 6 and makes similar arguments as those regarding claim 1. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claims 8-13 and 15 are allowable as they are dependent upon claim 6. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claim 37 is allowable as it contains limitations similar to claim 47. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Applicant argues that claims 38-46 are allowable as they are dependent upon claim 37. Examiner respectfully disagrees for reasons stated above with regards to claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-4, 6, 8-13 and 47-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al.

Regarding claim **1**, Trippe discloses a method of parallel processing bit-synchronous High-level Data Link Control data (see lines 1-5 of paragraph 23 on page 2), comprising: storing at least two bytes of bit-synchronous High-level Data Link Control data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); processing in parallel (see lines 1-5 of paragraph 23 on page 2) said current at least two bytes within said shift register so as to detect a start-of-frame sequence within said current at least two bytes in said shift register during a first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the start-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle); processing in parallel said current at least two bytes within said shift register so as to detect an end-of-frame sequence during at least one subsequent clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "end-of-frame" is the end-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle); and sending valid payload data bits to a packer logic unit (bit accumulator 338 in figure 5, for example), wherein said valid payload data bits comprise at least some bits shifted into said shift register between said start-of-frame sequence and said end-of-frame sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Similarly, regarding claim **6**, Trippe discloses a method of parallel processing bit-synchronous data (see lines 1-5 of paragraph 23 on page 2), comprising: storing at least two bytes of bit-synchronous data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); processing in parallel said current at least two bytes within said shift register so as to detect valid payload data bits within said current at least two bytes (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags); and storing detected valid payload data bits in a packer logic unit (bit accumulator 338 in figure 5, for example) for further processing (see paragraph 41 on page 3 which indicates some of the further processing).

Similarly, regarding claim **47**, Trippe discloses a bit-synchronous High-level Data Link Control engine (see title and lines 1-5 of paragraph 23 on page 2), comprising: a register for storing at least two bytes of bit-synchronous High-level Data Link Control data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); and a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, to detect valid payload data within said at least two bytes in said shift register, said de-framer unit detects a start-of-frame sequence within said at least two bytes during a first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the start-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and to detect an end-of-frame sequence during a subsequent clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example;

the "end-of-frame" is the end-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle), said valid payload data comprises at least some of the bits received between said start-of-frame sequence and said end-of-frame sequence (see paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags); and a packer logic unit, coupled to said de-framer unit, to store said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5), wherein said packer logic unit discards said valid payload data received from said de-framer unit if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Trippe does not disclose expressly the limitation that the High-level Data Link Control data is stored in a shift register, wherein, at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register of claim 1. Similarly, Trippe does not disclose the limitation of claim 6 that the bit-synchronous data is stored in a shift register, wherein a newly received byte is shifted in and an old byte is shifted out of said shift register at each clock cycle. Trippe also does not disclose the limitation that the register for storing at least two bytes of claim 47 is a shift register or that a new byte is shifted in and an old byte is shifted out of said shift register during each successive clock cycle. Trippe does not disclose the limitation of claims 1, 6, and 47 that said de-framer unit comprises a

plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register.

Stephenson, Jr. discloses the missing limitations of claims 1, 6, and 47 of a shift register (the three sequential latches) wherein at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register in lines 9-24 of column 6. Specifically, the passage starting on line 15 indicates that each data word causes the previous data words to be shifted over one latch. Stephenson, Jr. further discloses the limitation that the de-framer unit comprises a plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register in lines 24-49 of column 6 and in the example of figure 6. Clearly, successive 8-bit sequences of bits are scanned simultaneously to detect a given word (framing byte in this case).

Trippe and Stephenson, Jr. are analogous art because they are from the same field of endeavor of detecting byte patterns in bit sequences. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe by using the shift registers (latches) to store the High-level Data Link Control data while it is being analyzed and to further use the detectors as described by Stephenson, Jr. to simultaneously look at all successive 8-bit sequences in this shift register.

The motivation for doing so would have been allow the 8-bit framing bytes (start-of-frame, end-of-frame) to be detected regardless of the starting bit location of that byte as suggested by Stephenson, Jr. in lines 44-49 of column 6. Therefore, it would have been obvious

to combine Stephenson, Jr. with Trippe for the benefit of detecting framing bytes regardless of the starting bit location to obtain the invention as specified in claims 1, 6, and 47.

Regarding claims **2 and 48**, Trippe discloses processing in parallel said current at least two bytes within said shift register to detect an Abort sequence during said at least one subsequent clock cycle, wherein if said Abort sequence is detected, all bits received after said start-of-frame sequence are discarded and a search for a new start-of-frame sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (start-of-frame) when in the no-sync state.

Regarding claims **3 and 49**, Trippe discloses processing in parallel said current at least two bytes within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said start-of-frame sequence and said end-of-frame sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **4**, Trippe discloses discarding all bits received between said start-of-frame and end-of-frame sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **8**, Trippe discloses the limitation of searching for a start sequence within said shift register, wherein said valid payload data bits comprise at least some bits received after said start sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the start sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **9**, Trippe discloses the limitation of searching for an end sequence within said shift register, after said start sequence has been detected, during at least one clock cycle subsequent to said first clock cycle, wherein said valid payload data bits comprise at least some bits received between said start and end sequences in paragraph 35 of page 3, for example; the "end-of-frame" is the end sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **10**, Trippe discloses the limitation that said bit-synchronous data comprises bit-synchronous High-level Data Link Control data (see title and lines 1-5 of paragraph 23 on page 2), said start sequence comprises a start-of-frame sequence and said end sequence comprises an end-of-frame sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the start-of-frame sequence and "end-of-frame" is the end-of-frame sequence.

Regarding claim **11**, Trippe discloses the limitation of processing in parallel said current at least two bytes stored in said shift register to detect an Abort sequence during at least one clock cycle subsequent to said first clock cycle, wherein if said Abort sequence is detected, all bits received after said start-of-frame sequence are discarded and a search for a new start-of-

frame sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (start-of-frame) when in the no-sync state.

Regarding claim **12**, Trippe discloses the limitation of processing in parallel said current at least two bytes within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said start-of-frame sequence and said end-of-frame sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **13**, Trippe discloses the limitation of discarding all bits received between said start-of-frame and end-of-frame sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

5. Claims **37- 46, and 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al and in further view of U.S. Patent 5,465,345 to Blanc et al.

Regarding claim **37**, Trippe discloses a system for parallel processing bit-synchronous data (see lines 1-5 of paragraph 23 on page 2), comprising: a register to store a plurality of bits of

bit-synchronous data that comprises bit-synchronous High-level Data Link Control data, said register stores a current at least two bytes of said bit-synchronous High-level Data Link Control data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, to detect valid payload data, wherein said de-framer unit processes in parallel said current at least two bytes within said shift register during said clock cycles (see lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and searches for a start sequence comprised of a start-of-frame sequence and an end sequence within said shift register (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the start-of-frame sequence referred to in the claim), and said valid payload data bits comprise at least some bits received between said start-of-frame and end-of-frame sequences (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags); and a packer logic unit, coupled to said de-framer unit, to store said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5).

Similarly, regarding claim **44**, Trippe discloses a bit-synchronous High-level Data Link Control engine (see title and lines 1-5 of paragraph 23 on page 2), comprising: a register to store at least two bytes of bit-synchronous High-level Data Link Control data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); and a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, to detect valid payload data within said shift register, said de-

framer unit to detect a start-of-frame sequence during a first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the start-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and detects an end-of-frame sequence during a subsequent clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "end-of-frame" is the end-of-frame sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle), wherein said valid payload data comprises at least some of the bits received between said start-of-frame sequence and said end-of-frame sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags), and said de-framer unit further processes in parallel said current at least two bytes within said shift register to detect at least one stuff bit and discards said at least one stuff bit, if detected (see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said start-of-frame sequence and said end-of-frame sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags), excluding said at least one stuff bit (paragraphs 39 and 41 on page 3 indicate that the valid data forwarded does not include the stuff bits); and a packer logic unit, coupled to said de-framer unit, for storing said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5).

Trippe does not disclose expressly the limitation that the High-level Data Link Control data is stored in a shift register, wherein, at each successive clock cycle, a new incoming byte is

shifted into said shift register and an old byte is shifted out of said shift register of claims 37 and 44. Trippe does not disclose the limitation of claims 37 and 44 that said de-framer unit comprises a plurality, of comparators to detect a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register. Finally, Trippe does not disclose expressly the limitation that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Stephenson, Jr. discloses the limitations of claims 37 and 44 of a shift register wherein at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register in lines 9-24 of column 6. Specifically, the passage starting on line 15 indicates that each data word causes the previous data words to be shifted over one latch. Stephenson, Jr. further discloses the limitation that the de-framer unit comprises a plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register in lines 24-49 of column 6 and in the example of figure 6. Clearly, successive 8-bit sequences of bits are scanned simultaneously to detect a given word (framing byte in this case).

Trippe and Stephenson, Jr. are analogous art because they are from the same field of endeavor of detecting byte patterns in bit sequences. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe by using the shift registers

(latches) to store the High-level Data Link Control data while it is being analyzed and to further use the detectors as described by Stephenson, Jr. to simultaneously look at all successive 8-bit sequences in this shift register.

The motivation for doing so would have been allow the 8-bit framing bytes (start-of-frame, end-of-frame) to be detected regardless of the starting bit location of that byte as suggested by Stephenson, Jr. in lines 44-49 of column 6.

The combination of Trippe and Stephenson, Jr. does not disclose expressly the limitation that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Blanc discloses a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit in lines 25-38 of column 2 and lines 6-12 of column 8 which describe the zero delete table which is used to remove stuffed zeros from the High-level Data Link Control stream.

Trippe, modified by Stephenson, Jr., and Blanc are analogous art because they are from the same field of endeavor of HDLC bit stream processing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe, modified above, to further use a look up table such as the zero delete table in Blanc. The motivation for doing so would have been to provide faster processing as well as lower cost as suggested by Blanc in lines 33-38 of column 2. Therefore, it would have been obvious to combine Blanc with Trippe and

Stephenson, Jr. for the benefit of faster processing and lower cost to obtain the invention as specified in claims 37 and 44.

Regarding claim **38**, Trippe discloses discarding all bits received between said start-of-frame and end-of-frame sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **39**, Trippe discloses the limitation of searching for a specified sequence of bits stored within said shift register during a first clock cycle in paragraphs 9 and 10 on page 1, for example. See also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle.

Regarding claim **40**, Trippe discloses the limitation of searching for a start sequence within said shift register, wherein said valid payload data bits comprise at least some bits received after said start sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the start sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **41**, Trippe discloses the limitation of searching for an end sequence within said shift register, after said start sequence has been detected, during at least one subsequent clock cycle, wherein said valid payload data bits comprise at least some bits received

between said start and end sequences in paragraph 35 of page 3, for example; the "end-of-frame" is the end sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claims **42 and 46**, Trippe discloses processing in parallel said current at least two bytes within said shift register to detect an Abort sequence during said at least one subsequent clock cycle, wherein if said Abort sequence is detected, all bits received after said start-of-frame sequence are discarded and a search for a new start-of-frame sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (start-of-frame) when in the no-sync state.

Regarding claim **43**, Trippe discloses processing in parallel said current at least two bytes within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said start-of-frame sequence and said end-of-frame sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **45**, Trippe discloses a packer logic unit, coupled to said de-framer unit, to store said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5), wherein said packer logic unit to discard said valid payload data received from said de-framer unit if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator

outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **50**, the combination of Trippe and Stephenson, Jr. discloses the limitations of parent claim 47 as disclosed above. The combination of Trippe and Stephenson, Jr. does not disclose expressly the limitation of claim 50 that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Blanc discloses a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit in lines 25-38 of column 2 and lines 6-12 of column 8 which describe the zero delete table which is used to remove stuffed zeros from the HDLC stream.

Trippe, modified by Stephenson, Jr., and Blanc are analogous art because they are from the same field of endeavor of HDLC bit stream processing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe, modified above, to further use a look up table such as the zero delete table in Blanc. The motivation for doing so would have been to provide faster processing as well as lower cost as suggested by Blanc in lines 33-38 of column 2. Therefore, it would have been obvious to combine Blanc with Trippe and

Stephenson, Jr. for the benefit of faster processing and lower cost to obtain the invention as specified in claim 50.

6. Claim **15** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al and in further view of U.S. Patent 6,970,563 to Risling.

The combination of Trippe and Stephenson, Jr. discloses the limitations of parent claim 47 as disclosed above. The combination of Trippe and Stephenson, Jr. does not disclose expressly the limitation of claim 15 of de-scrambling said at least two bytes prior to storing said at least two bytes in said shift register, wherein said de-scrambling comprises de-scrambling at least eight bits in parallel during a single clock cycle.

However, Risling discloses this limitation in Figure 7 and lines 4-25 of column 7. Lines 4-7 indicate that in this embodiment, 32 bits are descrambled in parallel. Trippe, modified as above, and Risling are analogous art because they are from the same field of endeavor of fast (parallel) processing of serially transmitted data. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the above combination of Trippe and Stephenson, Jr. by descrambling the data stream prior to performing HDLC processing. The motivation for doing so would have been to allow the receiver to handle scrambled data in order to overcome the problems associated with sending an unbalanced number of 0s and 1s as well as to make the data unintelligible in case it is intercepted. This is suggested in lines 24-44 of column 1 of Risling. Therefore, it would have been obvious to combine Risling with Trippe as

modified by Stephenson, Jr. for the benefit of receiving scrambled data to obtain the invention as specified in claim 15.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Monday and Thursday from 7:00-5:30 Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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RCS 5-24-07

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5/24/07

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